We Claim:

1. An electronic device, comprising:

at least two semiconductor chips, each one of said semiconductor chips having an active top side with a plurality of contact areas;

a leadframe having a placement side and an edge region, said semiconductor chips integrated into said leadframe such that said placement side of said leadframe and said active top side of each one of said semiconductor chips are flush, said placement side of said leadframe and said active top side of each one of said semiconductor chips having a common fine wiring plane, said fine wiring plane having a plurality of contact pads configured in said edge region of said leadframe;

a rewiring substrate having a top side carrying said leadframe, said top side of said rewiring substrate having an edge region with a plurality of bonding areas, said rewiring substrate having an underside, said leadframe not covering said edge region of said rewiring substrate;

a plurality of bonding connections configured between said plurality of contact pads of said fine wiring plane of said leadframe and said plurality of bonding areas of said rewiring substrate;

a housing packaging said leadframe and said semiconductor chips; and

a plurality of external contacts distributed on said underside of said rewiring substrate.

2. The electronic device according to claim 1, wherein:

said semiconductor chips include a first semiconductor chip and a second semiconductor chip;

said first semiconductor chip has a thickness and said second semiconductor chip has a thickness that is different from said thickness of said first semiconductor chip;

said active top side of said first semiconductor chip has size and said active top side of said second semiconductor chip has size that is different from said size of said active top side of said first semiconductor chip; and

said first semiconductor chip has an integrated circuit and said second semiconductor chip has an integrated circuit that is different from said integrated circuit of said first semiconductor chip.

3. The electronic device according to claim 1, wherein:

each one of said semiconductor chips has a central bonding channel and a side edge with a plurality of outside contact areas;

said active top side of each one of said semiconductor chips has a plurality of arbitrarily distributed additional contact areas located outside said central bonding channel and outside said side edge.

4. The electronic device according to claim 1, wherein:

said fine wiring plane has a plurality of electrical interconnects configured between said plurality of contact areas of one of said semiconductor chips and said plurality of contact areas of another one of said semiconductor chips.

5. The electronic device according to claim 1, wherein:

said fine wiring plane has a plurality of electrical interconnects configured between said plurality of contact areas and said plurality of contact pads.

6. The electronic device according to claim 1, wherein:

said fine wiring plane has a plurality of thin-film interconnects.

7. The electronic device according to claim 1, wherein:

said fine wiring plane is configured with a plurality of passive discrete electronic components.

8. The electronic device according to claim 1, wherein:

said fine wiring plane has a plurality of thin-film components that are each selected from a group consisting of an electrical resistor, a comb filter, an inductive component and a capacitive component.

9. The electronic device according to claim 1, wherein:

said fine wiring plane has a plurality of electrical resistors with a meandering form.

10. The electronic device according to claim 1, wherein:

said fine wiring plane has a plurality of inductive components with a spiral form.

11. The electronic device according to claim 1, wherein:

said rewiring substrate has a plurality of rewiring lines and a plurality of passage contacts connected to said plurality of external contacts.

12. A leadframe configuration, comprising:

at least two semiconductor chips, each one of said semiconductor chips having an active top side with a plurality of contact areas; and

a leadframe having a placement side and an edge region;

said semiconductor chips integrated into said leadframe such that said placement side of said leadframe and said active top side of each one of said semiconductor chips are flush, said placement side of said leadframe and said active top side of each one of said semiconductor chips having a common fine wiring plane, said fine wiring plane having a plurality of contact pads configured in said edge region of said leadframe.

13. The leadframe configuration according to claim 12, wherein:

said fine wiring plane has a plurality of electrical interconnects configured between said plurality of contact

areas of one of said semiconductor chips and said plurality of contact areas of another one of said semiconductor chips.

14. The leadframe configuration according to claim 12, wherein:

said fine wiring plane has a plurality of electrical interconnects configured between said plurality of contact areas and said plurality of contact pads.

15. The leadframe configuration according to claim 12, wherein:

said fine wiring plane has a plurality of thin-film interconnects.

16. The leadframe configuration according to claim 12, wherein:

said fine wiring plane is configured with a plurality of passive discrete electronic components.

17. The leadframe configuration according to claim 12, wherein:

said fine wiring plane has a plurality of thin-film components that are each selected from a group consisting of an electrical resistor, a comb filter, an inductive component and a capacitive component.

18. The leadframe configuration according to claim 12, wherein:

said fine wiring plane has a plurality of electrical resistors with a meandering form.

19. The leadframe configuration according to claim 12, wherein:

said fine wiring plane has a plurality of inductive components with a spiral form.

20. A panel, comprising:

a plurality of leadframe positions;

each one of said plurality of leadframe positions having a leadframe configuration including:

at least two semiconductor chips, each one of said semiconductor chips having an active top side with a plurality of contact areas; and

a leadframe having a placement side and an edge region;

said semiconductor chips integrated into said leadframe such that said placement side of said leadframe and said active top side of each one of said semiconductor chips are flush, said placement side of said leadframe and said active top side of each one of said semiconductor chips having a common fine wiring plane, said fine wiring plane having a plurality of contact pads configured in said edge region of said leadframe.

21. The panel according to claim 20, wherein: said plurality of leadframe positions are configured in rows and columns.

22. The panel according to claim 21, wherein the panel has a panel member with a form and a size corresponding to a semiconductor wafer or to a printed circuit board.

23. A method for producing an electronic device, the method which comprises:

producing a first panel with a plurality of leadframe positions configured in rows and columns, each one of the plurality of leadframe positions having at least two semiconductor chips embedded in a material of the first panel such that a plurality of active top sides of the semiconductor chips are flush with a top side of the first panel;

applying a common fine wiring structure to the plurality of active top sides of the semiconductor chips and to the top side of the first panel in each of the plurality of leadframe positions, and configuring a plurality of contact pads in edge regions of the plurality of leadframe positions;

separating the first panel into a plurality of individual leadframes;

producing a rewiring plate with a plurality of device positions configured in rows and columns, configuring a plurality of bonding areas in edge regions of each of the plurality of device positions, and distributing a plurality of external contact areas on an underside of the rewiring plate in each one of the plurality of the device positions;

applying a leadframe separated from the first panel in each one of the plurality of device positions of the rewiring plate

while not covering the edge regions configured with the plurality of bonding areas;

producing a plurality of bonding connections between the plurality of contact pads in the edge regions of the plurality of leadframe positions and the plurality of bonding areas in the edge regions of each one of the plurality of device positions;

producing a second panel by covering the plurality of device positions with a plastic housing composition;

applying a plurality of external contacts on the plurality of external contact areas of the rewiring plate; and

separating the second panel into a plurality of individual electronic devices.

24. The method according to claim 23, which further comprises:

performing the step of applying the common fine wiring structure by using a photolithography method for finely patterning uniformly applied metal layers.

25. The method according to claim 23, which further comprises:

printing on a conductive paste and subsequently sintering the paste to form structures selected from a group consisting of interconnects, contact pads, bonding areas and passive components;

the structures used for a rewiring structure of the rewiring plate or a fine wiring structure of the first panel.

26. The method according to claim 23, which further comprises:

coating the plurality of contact pads in the edge regions of the plurality of leadframe positions with a bondable material.

27. The method according to claim 23, which further comprises:

performing the step of producing the plurality of bonding connections by thermocompression bonding a plurality of bonding wires on the plurality of the bonding areas and on the plurality of contact pads.

28. The method according to claim 23, which further comprises:

performing the step of covering the plurality of device positions with a plastic housing composition by using a transfer molding method.